WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor integrated circuit device comprising:

sequentially forming a gate insulating film, a conductor film containing silicon, and a cap insulating film containing a member capable of selectively etching a silicon nitride film in each of a first silicon semiconductor region and a second silicon semiconductor region;

patterning a laminated film constituted of the cap insulating film and the conductor film to form a gate electrode in each of the first and second silicon semiconductor regions;

using the laminated film as a mask for introducing impurity to selectively introduce the impurity so as to form source and drain diffusion regions in each of the first and the second silicon semiconductor regions;

forming a first silicon nitride film on a sidewall of each of the laminated films;

forming a second silicon nitride film on an entire surface;

depositing a first insulating film on the entire surface, and then leaving the first insulating film between the gate electrodes in the first silicon semiconductor region;

depositing a second insulating film in the second silicon semiconductor region, and then leaving the

second insulating film on a sidewall of each of the laminated films in the second silicon semiconductor region;

removing the second silicon nitride film on each of the laminated films and the second silicon nitride film left on a surface of the second silicon semiconductor region;

removing the cap insulating film left above each of the gate electrodes;

forming a metal silicide film on a surface of the conductor film of each of the gate electrodes and forming a metal silicide film on each surface of the source and drain diffusion regions formed in the second silicon semiconductor region; and

depositing a third silicon nitride film on the entire surface, and then leaving the third silicon nitride film on each of the gate electrodes.

2. The method according to claim 1, wherein when the gate electrodes are formed, a space between the gate electrodes formed in the second silicon semiconductor region is formed to be wider than a space between the gate electrodes formed in the first silicon semiconductor region.

3. The method according to claim 1, further comprising:

leaving the third silicon nitride film on each of the gate electrodes, and then depositing a third

insulating film on the entire surface;

flattening the third insulating film;

selectively etching the third insulating film to expose the surface of the source and drain diffusion regions formed in the second silicon semiconductor region; and

forming contact electrodes to connect with the surface of the source and drain diffusion regions.

4. The method according to claim 1, further comprising:

forming trench capacitors in the first silicon semiconductor region prior to sequentially forming the gate insulating film, the conductor film and the cap insulating film.

5. The method according to claim 1, wherein the conductor film is a polycrystalline silicon film into which the impurity is introduced.

6. The method according to claim 1, wherein the cap insulating film is formed by a chemical vapor deposition method.

7. The method according to claim 1, wherein the second silicon nitride film is formed by the chemical vapor deposition method.

8. The method according to claim 1, wherein the first insulating film is formed by the chemical vapor deposition method.

9. The method according to claim 1, wherein the

first insulating film is etched-back by a reactive ion etching technique, thereby leaving the first insulating film between the gate electrodes in the first silicon semiconductor region.

10. The method according to claim 1, wherein the first silicon semiconductor region is a p-well region provided on a semiconductor substrate, and the second silicon semiconductor region includes p- and n-well regions provided on the semiconductor substrate.

11. A semiconductor integrated circuit device comprising:

a pair of first gate electrodes including a conductor film which are each provided via a gate insulating film in a first silicon semiconductor region;

a first diffusion region provided in the first silicon semiconductor region between the pair of first gate electrodes;

first metal silicide films provided on upper surfaces of the pair of first gate electrodes respectively;

first silicon nitride films provided on the pair of first gate electrodes respectively;

second silicon nitride films provided respectively on sidewalls of a laminated film constituted of the pair of first gate electrodes and the first silicon nitride films;

a third silicon nitride film provided on the second silicon nitride film so that the first diffusion region is exposed in a flat portion positioned between the pair of first gate electrodes;

a self-aligned contact provided between the pair of first gate electrodes and electrically connected to the diffusion region;

a second gate electrode including a conductor film which is formed in a second silicon semiconductor region via a gate insulating film;

a pair of second diffusion regions formed in the second silicon semiconductor region positioned on both surfaces of the second gate electrode;

a second metal silicide film formed on an upper surface of the second gate electrode;

a fourth silicon nitride film provided on the second gate electrode;

a fifth silicon nitride film provided on a sidewall of a laminated film constituted of the second gate electrode and the fourth silicon nitride film;

a sixth silicon nitride film provided on the fifth silicon nitride film so as to extend onto a portion of the surface of the pair of second diffusion regions;

third metal silicide films provided respectively on the surfaces of the pair of second diffusion regions which are not covered with the sixth silicon nitride film;

an insulating film provided on the sixth silicon nitride film; and

a seventh silicon nitride film provided on the insulating film.

12. The semiconductor integrated circuit device according to claim 11, wherein trench capacitors are formed in the first silicon semiconductor region.

13. The semiconductor integrated circuit device according to claim 11, wherein the conductor film is a polycrystalline silicon film into which an impurity is introduced.